AAT2504

SystemPower™

Adjustable 3-Channel Regulator

General Description

The AAT2504 is a three-channel regulator consisting of a step-down converter with an input voltage range of 2.7V to 5.5V plus two low dropout (LDO) linear regulators. The two LDOs have an input voltage range of 1.8V to 5.5V, making them well-suited for post regulating from the step-down converter.

The step-down converter optimizes power efficiency throughout the load range. Pulling the MODE/SYNC pin high enables "PWM Only" operation, maintaining constant frequency and low output ripple across the operating range. Alternatively, the converter may be synchronized to an external clock to the MODE/ SYNC pin. The step-down converter delivers up to 800mA of output current. The switching frequency is 2MHz, minimizing the size of external components.

The two LDOs (LDOA/LDOB) have independent inputs and are capable of delivering up to 300mA each. Ultra low input voltage on the VLDOA and VLDOB pins (down to 1.62V) allows for efficient post-buck regulation. A Power-OK (POK) function provides an open drain output signal when LDOA is within regulation. Both LDOs feature low quiescent current and a low dropout voltage. The output voltages for both LDOs are adjustable to as low as 0.6V. The linear regulators have independent Enable pins. Typical no load quiescent current is a low 80µA when the step-down converter and LDOs are enabled.

The AAT2504 is available in a Pb-free 3x4mm QFN34-20 package and is rated over the -40°C to +85°C temperature range.

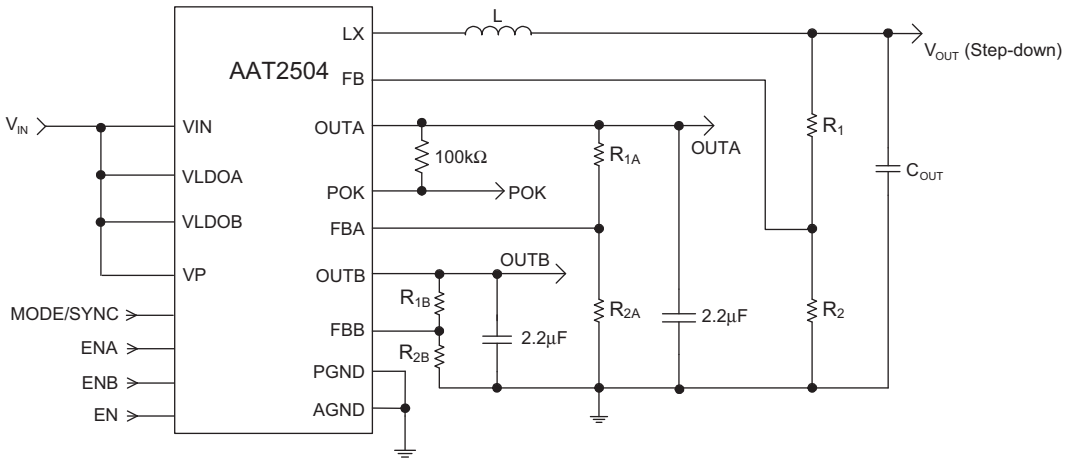
Features

- 800mA Buck Converter
  - V_{IN} Range: 2.7V to 5.5V
  - V_{OUT} Range: 0.9V to V_{IN}, Adjustable
  - High Efficiency: 95%
  - 2MHz Switching Frequency
  - Synchronizable to External Clock
  - Internal Soft Start
- Two 300mA Linear Regulators
  - LDO Input Voltage Range: 1.62V to 5.5V
  - Low Dropout Voltage
  - High Output Accuracy: ±1.5%
- Low Total Quiescent Current I_Q (80µA)
- Independent Enable Pins
- Over-Temperature Protection
- QFN34-20 Package
- -40°C to +85°C Temperature Range

Applications

- Cellular Phones
- Digital Cameras
- Handheld Instruments
- Microprocessor/DSP Core/IO Power
- PDAs and Handheld Computers

Typical Application

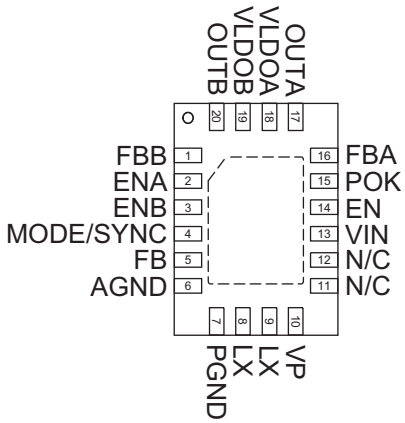


Pin Descriptions

Pin #	Symbol	Function
1	FBB	Feedback input pin for LDOB. This pin is used to regulate the output of LDOB to the desired value via an external resistor divider.
2	ENA	Enable pin for LDOA. Active high.
3	ENB	Enable pin for LDOB. Active high.
4	MODE/SYNC	PWM operation and oscillator synchronization pin. Connect to ground for PWM/Light Load operation and optimized efficiency throughout the load range. Connect high for low noise PWM operation under all operating conditions. When connected to an external clock, the internal oscillator is disabled and the step-down converter is synchronized to an external clock applied to this pin (PWM only).
5	FB	Feedback input pin for the step-down converter. This pin is used to see the output of the converter to regulate to the desired value via an external resistor divider.
6	AGND	Ground connection pin.
7	PGND	Main power ground return pin for the step-down converter. Connect to the output and input capacitor return.
8, 9	LX	Connect inductor to this pin. Switching node internally connected to the drain of both high- and low-side MOSFETs.
10	VP	Input supply voltage for the converter. Must be closely decoupled.
11, 12	N/C	Not connected.
13	VIN	Bias supply. Supply power for the internal circuitry. Connect to input power via low pass filter with de-coupling to AGND.
14	EN	Enable for the step-down converter. Active high.
15	POK	Power-OK pin with open drain output. It is pulled low when the OUTA pin is outside the regulation window. Place a pull-up resistor between POK and OUTA.
16	FBA	Feedback input pin for LDOA. This pin is used to regulate the output of LDOA to the desired value via an external resistor divider.
17	OUTA	LDOA output pin; should be closely decoupled with a low-ESR ceramic capacitor.
18	VLDOA	Input voltage pin for linear regulator A; should be closely decoupled.
19	VLDOB	Input voltage pin for linear regulator B; should be closely decoupled.
20	OUTB	LDOB output pin; should be closely decoupled with a low-ESR ceramic capacitor.
EP		Exposed paddle; connect to ground directly beneath the package.

Pin Configuration

QFN34-20
(Top View)



Absolute Maximum Ratings[1]

Symbol	Description	Value	Units
V_P, V_{IN}, V_{LDO}	Input Voltage and Bias Power to GND	6.0	V
V_{LX}	LX to GND	-0.3 to V_P + 0.3	V
V_{FB}	FB to GND	-0.3 to V_P + 0.3	V
V_{EN}	EN and EN_LDO to GND	-0.3 to 6.0	V
T_J	Operating Junction Temperature Range	-40 to 150	°C
T_{LEAD}	Maximum Soldering Temperature (at leads, 10 sec)	300	°C

Thermal Information

Symbol	Description	Value	Units
P_D	Maximum Power Dissipation (T_A = 25°C)	2.0	W
θ_{JA}	Thermal Resistance[2]	50	°C/W

1. Stresses above those listed in Absolute Maximum Ratings may cause permanent damage to the device. Functional operation at conditions other than the operating conditions specified is not implied. Only one Absolute Maximum Rating should be applied at any one time.
2. Mounted on an FR4 board.

Electrical Characteristics[1]

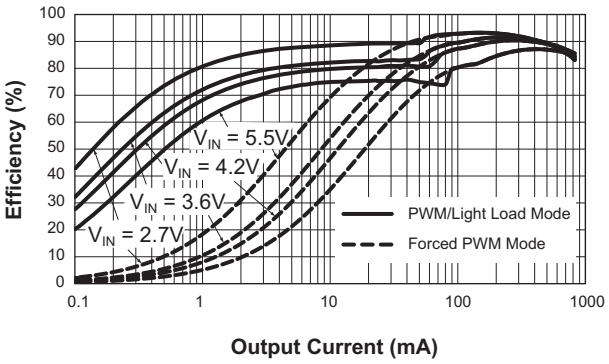
V_{IN} = 3.6V; T_A = -40°C to +85°C, unless otherwise noted. Typical values are T_A = 25°C.

Symbol	Description	Conditions		Min	Typ	Max	Units
Bias Power Supply							
I_Q	Quiescent Current	ENA = ENB = EN = V_{IN}; I_{LOAD} = 0			80	145	µA
I_{SHDN}	Shutdown Current	ENA = ENB = EN = GND				1.0	µA
UVLO	Under-Voltage Lockout Voltage	V_{IN} Rising				2.2	V
		Hysteresis			250		mV
		V_{IN} Falling		1.7			V
LDOA, LDOB							
V_{LDO}	Input Voltage			1.62		5.5	V
V_{OUT}	Output Voltage Tolerance	I_{OUT} = 1mA to 300mA	T_A = 25°C	-1.5		1.5	%
			T_A = -40°C to +85°C	-2.5		2.5	
V_{FB}	Feedback Voltage			0.593	0.6	0.607	V
V_{DO}	Dropout Voltage[2, 3]	I_{OUT} = 300mA				300	mV
$\Delta V_{LINEREG}/V_{IN}$	Line Regulation[4]	V_{IN} = V_{OUT} + 1 to 5.0V				0.09	%/V
$V_{EN(L)}$	Enable Threshold Low					0.6	V
$V_{EN(H)}$	Enable Threshold High			1.4			V
I_{OUT}	Output Current	$V_{LDO\ (MIN)}$ = 2.5		300			mA
I_{SHT}	Shutdown Current	V_{IN} = 5V				1.0	µA
T_{SD}	Over-Temperature Shutdown Threshold				140		°C
T_{HYS}	Over-Temperature Shutdown Hysteresis				15		°C
LDOA							
V_{POK}	Power-OK Trip Threshold	V_{OUT} Rising, T_A = 25°C		80	90	98	% of V_{OUT}
V_{POKHYS}	Power-OK Hysteresis				1.0		% of V_{OUT}
$V_{POK(LO)}$	Power-OK Output Voltage Low	I_{SINK} = 1mA				0.4	V
I_{POK}	Power-OK Output Leakage Current	V_{POK} <5.5V, V_{OUT} in Regulation				1.0	µA
Step-Down Converter							
V_{IN}	Input Voltage			2.7		5.5	V
V_{OUT}	Output Voltage Tolerance	I_{OUT} = 0 to 800mA; V_{IN} = 2.7V to 5.5V		-3.0		3.0	%
V_{OUT}	V_{OUT} Programmable Range			0.9		V_{IN}	V
V_{FB}	Feedback Threshold Voltage			0.891	0.9	0.909	V
I_{SHDN}	Shutdown Current	EN = GND				1.0	µA
I_{LX_LEAK}	LX Leakage Current	V_{IN} = 5.5, V_{LX} = 0 - V_{IN}				1.0	µA
I_{FB}	Feedback Leakage	V_{FB} = 1.0V				0.2	µA
I_{LIM}	Current Limit					1.2	A
$R_{DS(ON)H}$	High Side Switch On Resistance				280		mΩ
$R_{DS(ON)L}$	Low Side Switch On Resistance				160		mΩ
$\Delta V_{LOADREG}/V_{OUT}$	Load Regulation	I_{LOAD} = 10 to 800mA			0.2		%
$\Delta V_{LINEREG}/V_{IN}$	Line Regulation				0.2		%/V
F_{OSC}	Oscillator Frequency			1.6	2.0	2.4	MHz
T_{SD}	Over-Temperature Shutdown Threshold				140		°C
T_{HYS}	Over-Temperature Shutdown Hysteresis				15		°C
$V_{EN(L)}$	Enable Threshold Low					0.6	V
$V_{EN(H)}$	Enable Threshold High			1.4			V
I_{EN}	EN Input Leakage	V_{EN} = 5V, V_{IN} = 5V		-1.0		1.0	µA

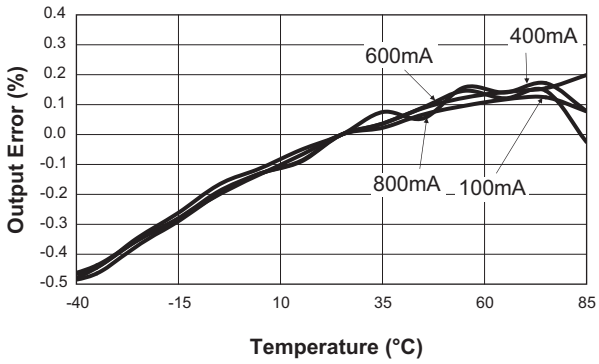
1. The AAT2504 is guaranteed to meet performance specifications over the -40°C to +85°C operating temperature range and is assured by design, characterization, and correlation with statistical process controls.
2. V_{DO} is defined as V_{IN} - V_{OUT} when V_{OUT} is 98% of nominal.
3. For V_{OUT} < 1.5V, V_{DO} = 1.8 - V_{OUT}.
4. C_{IN} = 10µF.

Typical Characteristics–Step-Down Converter

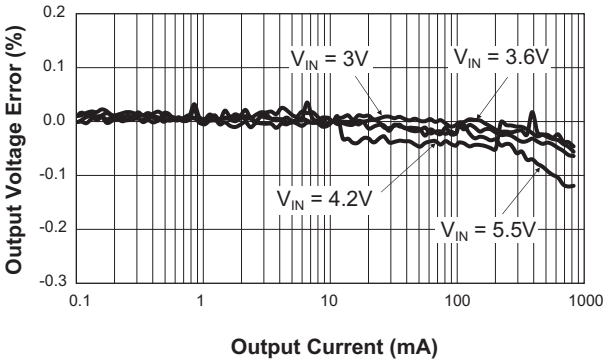
Step-Down Converter Efficiency vs. Output Current
(V_{OUT} = 1.8V)



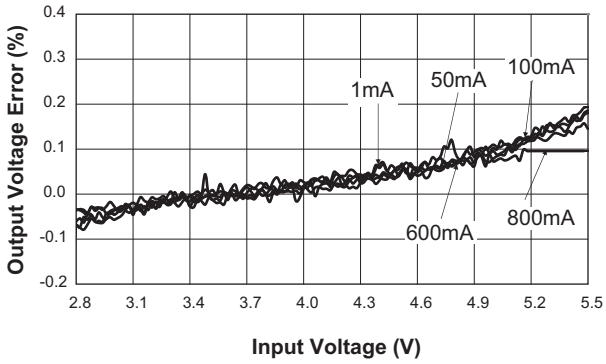
Output Voltage Error vs. Temperature
(V_{IN} = 3.6V; V_{OUT} = 2.5V)



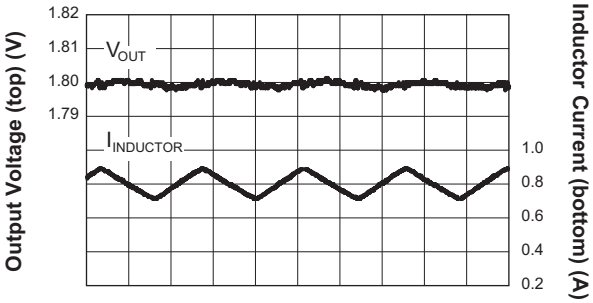
Step-Down Converter Load Regulation
(V_{OUT} = 2.5V; Forced PWM)



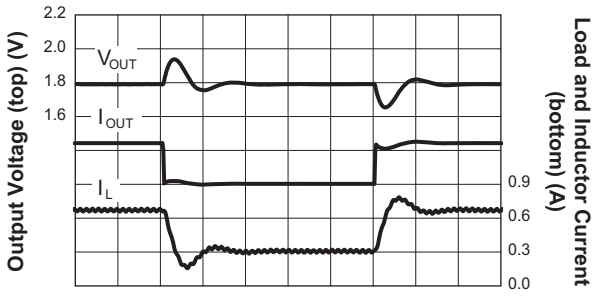
Step-Down Converter Line Regulation
(V_{OUT} = 2.5V; Forced PWM)



Step-Down Converter Output Ripple
(V_{IN} = 3.6V; V_{OUT} = 1.8V; I_{OUT} = 800mA)

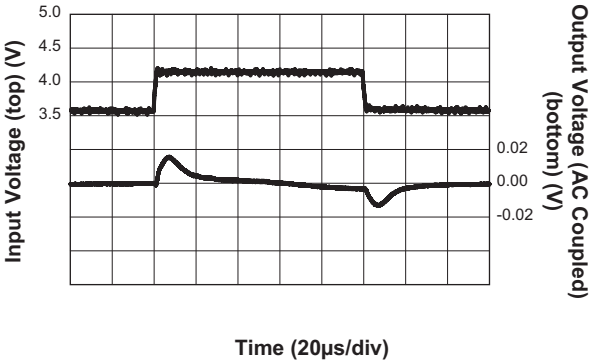


Step-Down Converter Load Transient
(V_{IN} = 3.6V; I_{OUT} = 300mA to 650mA)

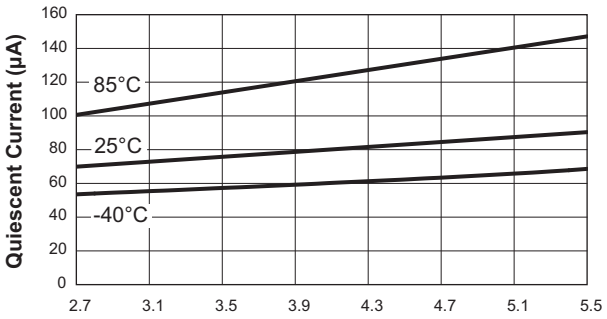


Typical Characteristics–Step-Down Converter

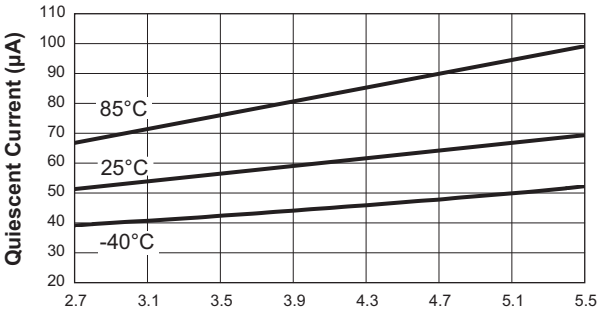
Step-Down Converter Line Transient
(V_{OUT} = 1.8V; I_{OUT} = 800mA; V_{IN} = 3.6V-4.2V)



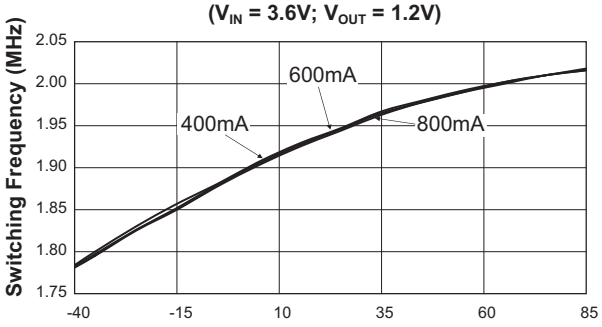
No Load Quiescent Current vs. Input Voltage
(Step-Down Converter Enabled; Both LDOs Enabled)



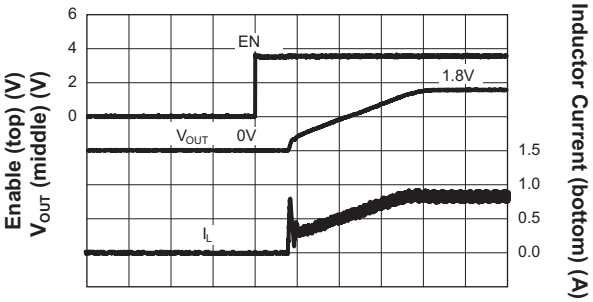
No Load Quiescent Current vs. Input Voltage
(Step-Down Converter Enabled; Both LDOs Disabled)



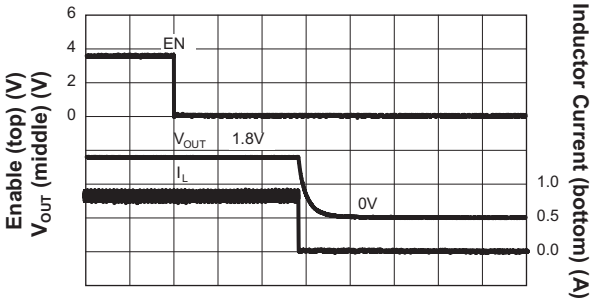
Step-Down Converter Switching Frequency vs. Temperature
(V_{IN} = 3.6V; V_{OUT} = 1.2V)



Step-Down Converter Soft Start
(V_{IN} = 3.6V; V_{OUT} = 1.8V; I_{OUT} = 800mA)

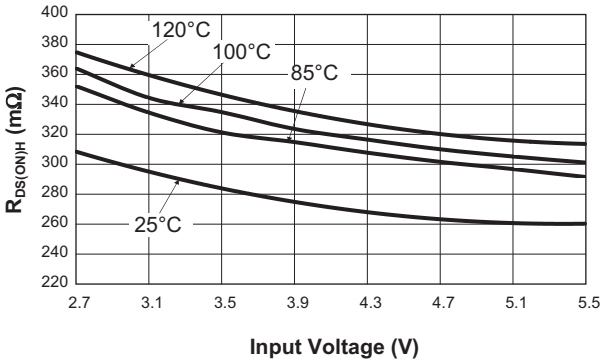


Step-Down Converter Turn-Off
(V_{IN} = 3.6V; V_{OUT} = 1.8V; I_{OUT} = 800mA)

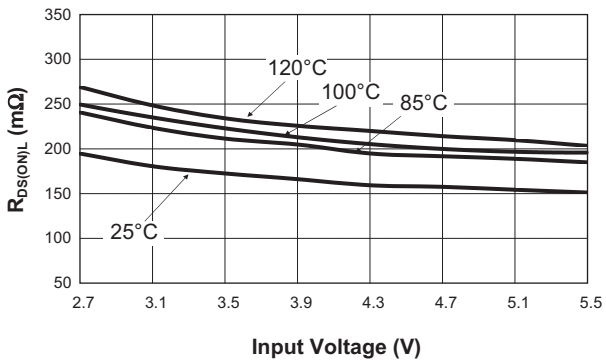


Typical Characteristics–Step-Down Converter

High Side Switch On Resistance vs. Input Voltage

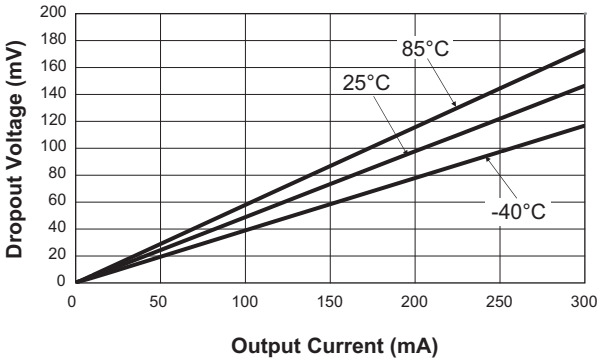


Low Side Switch On Resistance vs. Input Voltage

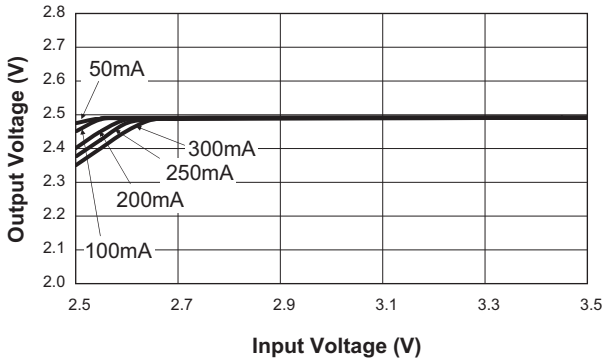


Typical Characteristics–LDO Regulator

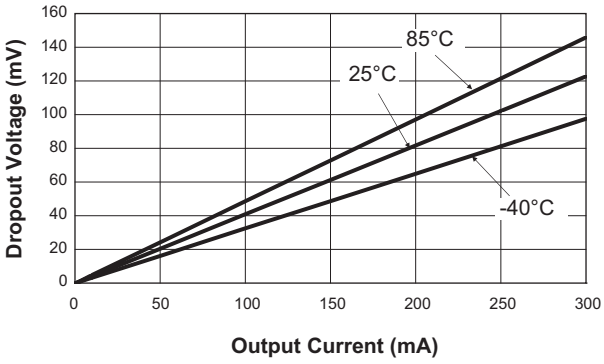
Dropout Voltage vs. Output Current
(V_{OUT} = 2.5V)



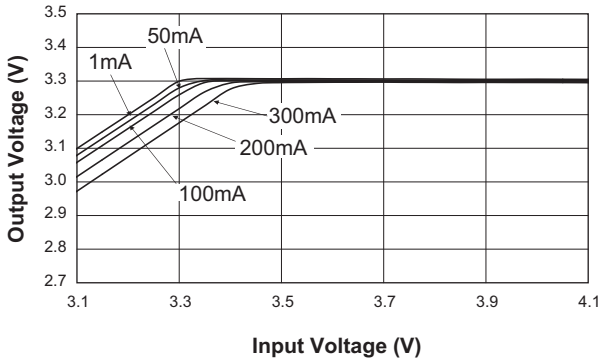
Output Voltage vs. Input Voltage
(V_{OUT} = 2.5V)



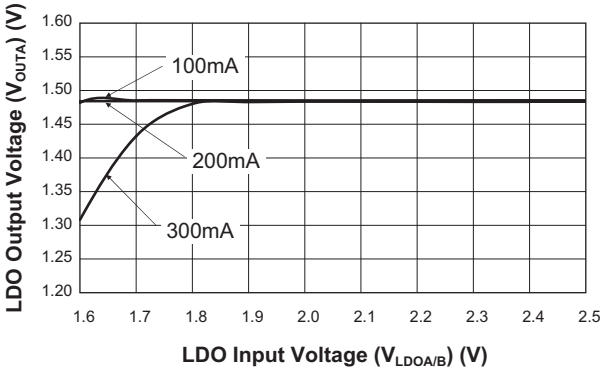
Dropout Voltage vs. Output Current
(V_{OUT} = 3.3V)



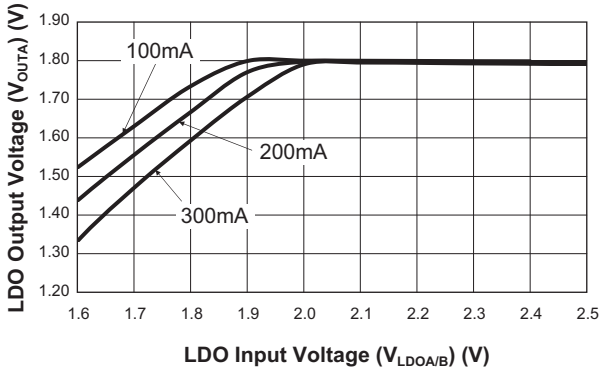
Output Voltage vs. Input Voltage
(V_{OUT} = 3.3V)



LDO Output Voltage vs. LDO Input Voltage
(V_{OUTA} = 1.5V; V_{IN} = V_P = 3.6V)

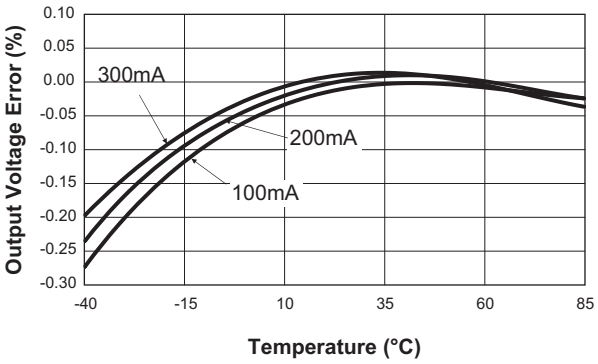


LDO Output Voltage vs. LDO Input Voltage
(V_{OUTA} = 1.8V; V_{IN} = V_P = 3.6V)

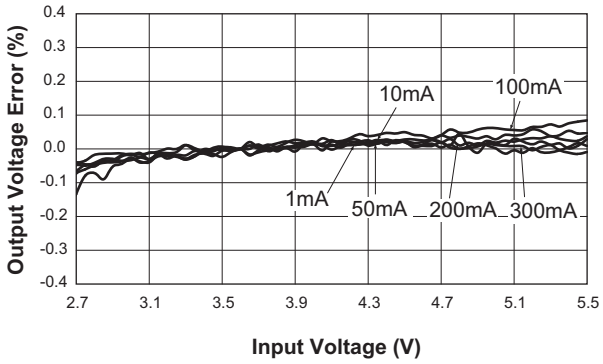


Typical Characteristics–LDO Regulator

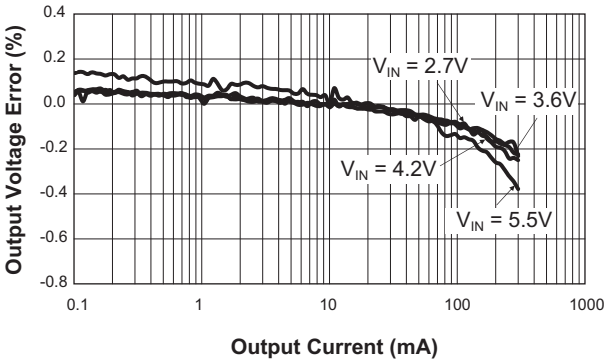
LDO Output Voltage Variation vs. Temperature
(V_{OUT} = 2.5V)



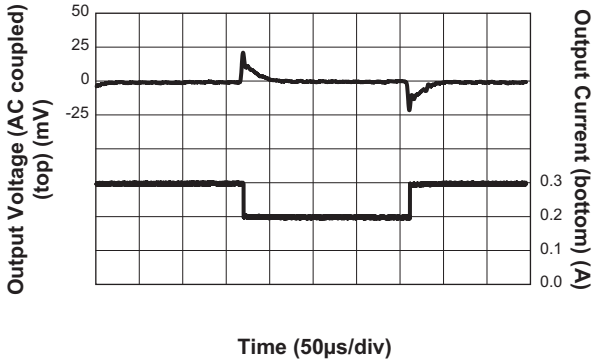
LDO Line Regulation
(V_{OUT} = 2.5V)



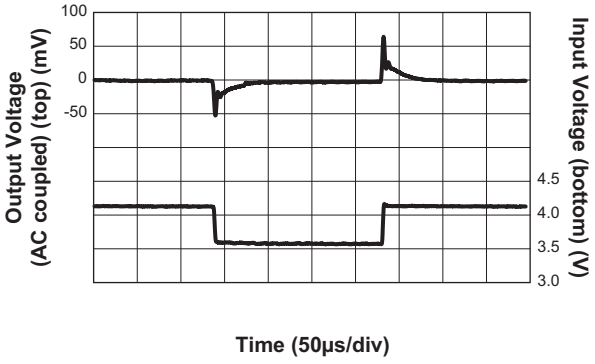
LDO Load Regulation
(V_{OUT} = 2.5V)



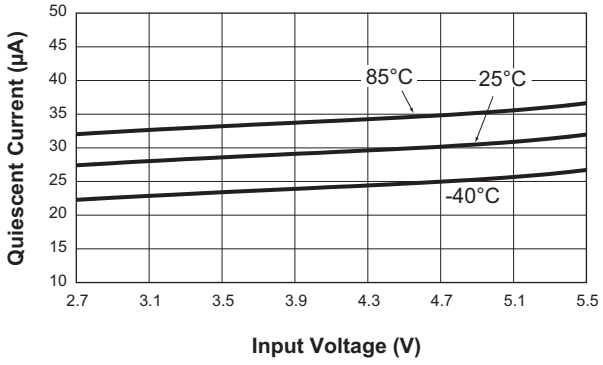
LDO Load Transient
(V_{OUT} = 1.8V)



LDO Line Transient
(V_{OUT} = 1.8V; I_{OUT} = 300mA)

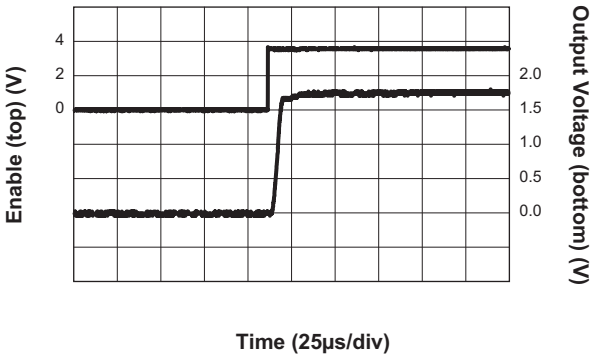


No Load Quiescent Current vs. Input Voltage
(Both LDOs Enabled, Step-Down Converter Disabled)

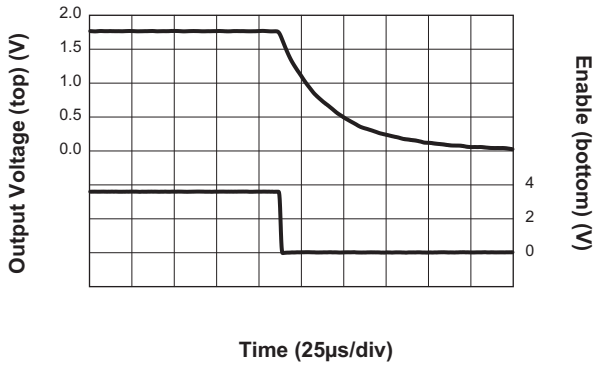


Typical Characteristics–LDO Regulator

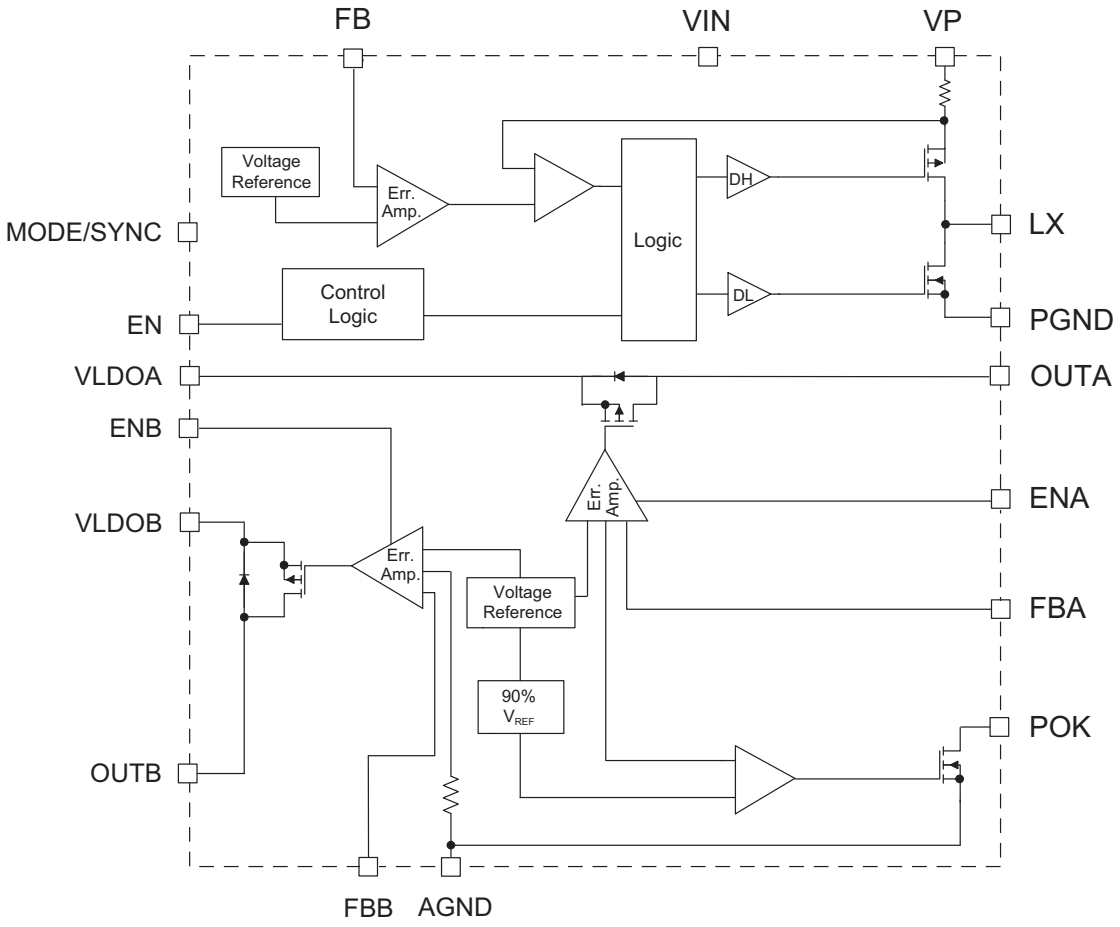
Turn-On Time
(V_{IN} = 3.6V; V_{OUT} = 1.8V; I_{OUT} = 300mA)



Turn-Off Time
(V_{IN} = 3.6V; V_{OUT} = 1.8V; I_{OUT} = 300mA)



Functional Block Diagram



Functional Description

The AAT2504 is a high performance power management IC comprised of a step-down converter and two linear regulators. The step-down converter operates in both fixed and variable frequency modes for high efficiency performance. The switching frequency is 2MHz, minimizing the size of the inductor. The converter requires only three external power components (C_{IN}, C_{OUT}, and L). Each LDO can deliver up to 300mA. Each regulator has independent input voltage and enable pins and operates with ceramic capacitors.

Switch-Mode Step-Down Converter

The switching regulator is a monolithic step-down converter operating with input voltage range of 2.7V to 5.5V. Power devices are sized for 800mA current capability and achieves over 95% efficiency. The internal oscillator operates at 2MHz, minimizing the cost and size of external components. Light Load operation maintains high efficiency under light load conditions (typically <50mA) when MODE/SYNC is grounded. The MODE/SYNC pin tied high allows optional "PWM Only" operation. This maintains constant frequency and low output ripple across all load conditions. Alternatively, by connecting an external clock to the AAT2504's MODE/SYNC pin, the internal clock is disabled. The external synchronization must stay between 1MHz and 3MHz.

The current through the P-channel MOSFET (high side) is sensed for current loop control, as well as short-circuit and overload protection. A fixed slope compensation signal is added to the sensed current to maintain stability for duty cycles greater than 50%. The peak current mode loop appears as a voltage-programmed current source in parallel with the output capacitor.

The output of the voltage error amplifier programs the current mode loop for the necessary peak switch current to force a constant output voltage for all load and line conditions. Internal loop compensation terminates the transconductance voltage error amplifier output. The internal error amplifier reference is fixed at 0.9V.

A logic low on the EN pin shuts the converter down and makes it consume less than 1µA of current.

Soft start increases the inductor current limit point in discrete steps when the input voltage or enable input is applied. It limits the current surge seen at the input and eliminates output voltage overshoot.

For overload conditions, the peak input current is limited. As load impedance decreases and the output voltage falls closer to zero, more power is dissipated internally, raising the device temperature. Thermal protection completely disables switching when internal dissipation becomes excessive, protecting the device from damage. The junction over-temperature threshold is 140°C with 15°C of hysteresis.

Linear Regulators

The two linear regulators are high performance LDOs where each LDO sources 300mA of current. For added flexibility, both regulators have independent input voltages operating from 1.8V to 5.5V. An external feedback pin for each LDO allows programming the output voltage from 3.6V to 0.6V. The regulators have thermal protection in case of adverse operating conditions.

LDOA features an integrated Power-OK comparator which indicates when the output is out of regulation. The POK is an open drain output and it is held low when the AAT2504 is in shutdown mode.

Under-Voltage Lockout

Internal bias of all circuits is controlled via the VIN pin. Under-voltage lockout guarantees sufficient V_{IN} bias and proper operation of all internal circuits prior to activation.

Over-Temperature Protection

Thermal protection completely disables switching when internal dissipation becomes excessive. The junction over-temperature threshold is 140°C with 15°C of hysteresis. Once an over-temperature fault condition is removed, the output voltage automatically recovers.

Applications Information

Step-Down Converter Inductor Selection

The step-down converter uses peak current mode control with slope compensation to maintain stability for duty cycles greater than 50%. The output inductor value must be selected so the inductor current down slope meets the internal slope compensation requirements. The internal slope compensation for the AAT2504 step-down converter is 0.51A/µs. This equates to a slope compensation that is 75% of the inductor current down slope for a 1.5V output and 2.2µH inductor.

$$m = \frac{0.75 \cdot V_O}{L} = \frac{0.75 \cdot 1.5V}{2.2\mu H} = 0.51 \frac{A}{\mu s}$$

Manufacturer's specifications list both the inductor DC current rating, which is a thermal limitation, and the peak current rating, which is determined by the saturation characteristics. The inductor should not show any appreciable saturation under normal load conditions. Some inductors may meet the peak and average current ratings yet result in excessive losses due to a high DCR. Always consider the losses associated with the DCR and its effect on the total converter efficiency when selecting an inductor.

The 2.2µH CDRH2D14 series Sumida inductor has a 94mΩ DCR and a 1.5A DC current rating. At full 800mA load, the inductor DC loss is 60mW which gives a 4.16% loss in efficiency for a 800mA, 1.8V output.

Input Capacitor

Select a 4.7µF to 10µF X7R or X5R ceramic capacitor for the input of the step-down converter. To estimate the required input capacitor size, determine the acceptable input ripple level (V_{PP}) and solve for C_{IN}. The calculated value varies with input voltage and is a maximum when V_{IN} is double the output voltage.

$$C_{IN} = \frac{\frac{V_O}{V_{IN}} \cdot \left(1 - \frac{V_O}{V_{IN}}\right)}{\left(\frac{V_{PP}}{I_O} - ESR\right) \cdot F_S}$$

$$\frac{V_O}{V_{IN}} \cdot \left(1 - \frac{V_O}{V_{IN}}\right) = \frac{1}{4} \text{ for } V_{IN} = 2 \cdot V_O$$

$$C_{IN(MIN)} = \frac{1}{\left(\frac{V_{PP}}{I_O} - ESR\right) \cdot 4 \cdot F_S}$$

Always examine the ceramic capacitor DC voltage coefficient characteristics when selecting the proper value. For example, the capacitance of a 10µF, 6.3V, X5R ceramic capacitor with 5.0V DC applied is actually about 6µF.

The maximum input capacitor RMS current is:

$$I_{RMS} = I_O \cdot \sqrt{\frac{V_O}{V_{IN}} \cdot \left(1 - \frac{V_O}{V_{IN}}\right)}$$

The input capacitor RMS ripple current varies with the input and output voltage and will always be less than or equal to half of the total DC load current.

$$\sqrt{\frac{V_O}{V_{IN}} \cdot \left(1 - \frac{V_O}{V_{IN}}\right)} = \sqrt{D \cdot (1 - D)} = \sqrt{0.5^2} = \frac{1}{2}$$

for $V_{IN} = 2 \cdot V_O$:

$$I_{RMS(MAX)} = \frac{I_O}{2}$$

The term $\frac{V_O}{V_{IN}} \cdot \left(1 - \frac{V_O}{V_{IN}}\right)$ appears in both the input voltage ripple and input capacitor RMS current equations and is a maximum when V_O is twice V_{IN}. This is why the input voltage ripple and the input capacitor RMS current ripple are a maximum at 50% duty cycle.

The input capacitor provides a low impedance loop for the edges of pulsed current drawn by the AAT2504. Low ESR/ESL X7R and X5R ceramic capacitors are ideal for this function. To minimize stray inductance, the capacitor should be placed as closely as possible to the IC. This keeps the high frequency content of the input current localized, minimizing EMI and input voltage ripple.

A laboratory test set-up typically consists of two long wires running from the bench power supply to the evaluation board input voltage pins. The inductance of these wires, along with the low-ESR ceramic input capacitor, can create a high Q network that may affect converter performance. This problem often becomes apparent in the form of excessive ringing in the output voltage during load transients. Errors in the loop phase and gain measurements can also result.

Since the inductance of a short PCB trace feeding the input voltage is significantly lower than the power leads from the bench power supply, most applications do not exhibit this problem.

In applications where the input power source lead inductance cannot be reduced to a level that does not affect the converter performance, a high ESR tantalum or aluminum electrolytic should be placed in parallel with the low ESR, ESL bypass ceramic. This dampens the high Q network and stabilizes the system.

Configuration	Output Voltage	Inductor
0.9V Adjustable With External Feedback	1V, 1.2V	1.5µH
	1.5V, 1.8V	2.2µH
	2.5V, 3.3V	3.3µH

Table 1: Inductor Values.

Output Capacitor

The output capacitor limits the output ripple and provides holdup during large load transitions. A 4.7µF to 10µF X5R or X7R ceramic capacitor typically provides sufficient bulk capacitance to stabilize the output during large load transitions and has the ESR and ESL characteristics necessary for low output ripple.

The output voltage droop due to a load transient is dominated by the capacitance of the ceramic output capacitor. During a step increase in load current, the ceramic output capacitor alone supplies the load current until the loop responds. Within two or three switching cycles, the loop responds and the inductor current increases to match the load current demand. The relationship of the output voltage droop during the three switching cycles to the output capacitance can be estimated by:

$$C_{OUT} = \frac{3 \cdot \Delta I_{LOAD}}{V_{DROOP} \cdot F_S}$$

Once the average inductor current increases to the DC load level, the output voltage recovers. The above equation establishes a limit on the minimum value for the output capacitor with respect to load transients.

The internal voltage loop compensation also limits the minimum output capacitor value to 4.7µF. This is due to its effect on the loop crossover frequency (bandwidth), phase margin, and gain margin. Increased output capacitance will reduce the crossover frequency with greater phase margin.

Adjustable Output Resistor Selection

The output voltage on the step-down converter is programmed with external resistors R2 and R6. To limit the bias current required for the external feedback resistor string while maintaining good noise immunity, the minimum suggested value for R6 is 59kΩ. Although a larger value will further reduce quiescent current, it will also

increase the impedance of the feedback node, making it more sensitive to external noise and interference. Table 2 summarizes the resistor values for various output voltages with R6 set to either 59kΩ for good noise immunity or 221kΩ for reduced no load input current.

With enhanced transient response for extreme pulsed load application, an external feed-forward capacitor (C1 in Fig.3) can be added.

V_{OUT} (V)	R6 = 59kΩ R2 (kΩ)	R6 = 221kΩ R2 (kΩ)
0.9*	0	0
1.0	6.65	24.3
1.1	13.3	48.7
1.2	19.6	73.2
1.3	26.1	97.6
1.4	32.4	124
1.5	39.2	147
1.8	59.0	221
1.85	61.9	232
2.0	71.5	274
2.5	105	392
2.8	124	464
3.0	137	511
3.3	158	590

Table 2: Step-Down Converter Resistor Values for Various Output Voltages.

Thermal Calculations

There are three types of losses associated with the AAT2504 step-down converter: switching losses, conduction losses, and quiescent current losses. Conduction losses are associated with the $R_{DS(ON)}$ characteristics of the power output switching devices. Switching losses are dominated by the gate charge of the power output switching devices. At full load, assuming continuous conduction mode (CCM), a simplified form of the LDO losses is given by:

$$P_{TOTAL} = \frac{I_O^2 \cdot (R_{DSON(HS)} \cdot V_O + R_{DSON(LS)} \cdot [V_{IN} - V_O])}{V_{IN}}$$

$$+ (t_{sw} \cdot F \cdot I_O + I_Q) \cdot V_{IN}$$

I_Q is the step-down converter quiescent current. The term t_{sw} is used to estimate the full load step-down converter switching losses.

For the condition where the step-down converter is in dropout at 100% duty cycle, the total device dissipation reduces to:

$$P_{TOTAL} = I_O^2 \cdot R_{DSON(HS)} + I_Q \cdot V_{IN}$$

Since $R_{DS(ON)}$, quiescent current, and switching losses all vary with input voltage, the total losses should be investigated over the complete input voltage range.

Given the total losses, the maximum junction temperature can be derived from the θ_{JA} for the QFN34-20 package which is 50°C/W.

$$T_{J(MAX)} = P_{TOTAL} \cdot \Theta_{JA} + T_{AMB}$$

LDO Linear Regulator Input Capacitor

A 1µF or larger capacitor is typically recommended for C_{IN} in most applications. A C_{IN} capacitor is not required for basic LDO regulator operation; however, if the AAT2504 is physically located more than three centimeters from an input power source, a C_{IN} capacitor will be needed for stable operation. C_{IN} should be located as closely to the device VLDO pins as practically possible. C_{IN} values greater than 1µF will offer superior input line transient response and will assist in maximizing the highest possible power supply ripple rejection.

Ceramic, tantalum, or aluminum electrolytic capacitors may be selected for C_{IN}. There is no specific capacitor ESR requirement for C_{IN}; however, ceramic capacitors are recommended for C_{IN} due to their inherent capability over tantalum capacitors to withstand input current surges from low impedance sources such as batteries in portable devices.

Output Capacitor

For proper load voltage regulation and operational stability, a capacitor is required between pins OUTA, OUTB, and GND. The C_{OUT} capacitor connection to the LDO regulator ground pin should be made as direct as practically possible for maximum device performance. The AAT2504 has been specifically designed to function with very low ESR ceramic capacitors. For best performance, ceramic capacitors are recommended.

* For the 0.9V output, R6 is open.

Typical output capacitor values for maximum output current conditions range from 1µF to 10µF.

Applications utilizing the exceptionally low output noise and optimum power supply ripple rejection characteristics of the AAT2504 should use 2.2µF or greater for C_{OUT}. If desired, C_{OUT} may be increased without limit. In low output current applications where output load is less than 10mA, the minimum value for C_{OUT} can be as low as 0.47µF.

Capacitor Characteristics

Ceramic composition capacitors are highly recommended over all other types of capacitors for use with the AAT2504. Ceramic capacitors offer many advantages over their tantalum and aluminum electrolytic counterparts. A ceramic capacitor typically has very low ESR, is lower cost, has a smaller PCB footprint, and is non-polarized. Line and load transient response of the LDO regulator is improved by using low ESR ceramic capacitors. Since ceramic capacitors are non-polarized, they are not prone to incorrect connection damage.

Equivalent Series Resistance

ESR is a very important characteristic to consider when selecting a capacitor. ESR is the internal series resistance associated with a capacitor that includes lead resistance, internal connections, size and area, material composition, and ambient temperature. Typically, capacitor ESR is measured in milliohms for ceramic capacitors and can range to more than several ohms for tantalum or aluminum electrolytic capacitors.

Ceramic Capacitor Materials

Ceramic capacitors less than 0.1µF are typically made from NPO or C0G materials. NPO and C0G materials generally have tight tolerance and are very stable over temperature. Larger capacitor values are usually composed of X7R, X5R, Z5U, or Y5V dielectric materials. NPO and C0G material types are not recommended for use with LDO regulators since the capacitor tolerance can vary more than ±50% over the operating temperature range of the device. A 2.2µF Y5V capacitor could be reduced to 1µF over temperature; this could cause problems for circuit operation. X7R and X5R dielectrics are much more desirable. The temperature tolerance of X7R dielectric is better than ±15%. Capacitor area is another contributor to ESR. Capacitors which are physically large in size will have a lower ESR when compared to a smaller sized capacitor of an equivalent material and capacitance value. These larger devices can improve circuit transient response when compared to an equal value capacitor in a smaller package size. Consult capacitor vendor datasheets carefully when selecting capacitors for LDO regulators.

Adjustable Output Resistor Selection

The output voltage on the linear regulator is programmed with external resistors: R4 and R7 for LDOA and R5 and R8 for LDOB. Table 3 summarizes the resistor values for various output voltages with R4 and R5 set to either 59kΩ for good noise immunity or 221kΩ for reduced no load input current.

LDO V_{OUT} (V)	R7, R8 = 59kΩ R4, R5 (kΩ)	R7, R8 = 221kΩ R4, R5 (kΩ)
0.6*	0	0
0.8	19.6	75
0.9	29.4	113
1.0	39.2	150
1.1	49.9	187
1.2	59.0	221
1.3	68.1	261
1.4	78.7	301
1.5	88.7	332
1.8	118	442
1.85	124	464
2.0	137	523
2.5	187	715
3.3	267	1000

Table 3: LDO Linear Regulators Resistor Values for Various Output Voltages.

POK Output

LDOA of the AAT2504 features an integrated Power OK comparator which can be used as an error flag. The POK open drain output goes low when output voltage is 10% (typ) below its nominal regulation voltage. Additionally, any time LDOA is in shutdown, the POK output is pulled low. Connect a pull-up resistor from POK to OUTA.

*For the 0.6V output, R7 and R8 are open.

Enable Function

The AAT2504 features an LDO regulator enable/disable function. Each LDO has its own dedicated enable pin. These pins (ENA, ENB) are active high and are compatible with CMOS logic. To assure the LDO regulators will switch on, ENA/B must be greater than 1.4V. The LDO regulators will shut down when the voltage on the ENA/B pins falls below 0.6V. In shutdown, the LDO regulators will consume less than 1.0µA of current. If the enable function is not needed in a specific application, it may be tied to V_{IN} to keep the LDO regulator in a continuously on state.

Thermal Protection

Each of the two LDOs of the AAT2504 has an internal thermal protection circuit which will turn on when the device die temperature exceeds 140°C. The LDO regulator outputs will remain in a shutdown state until the internal die temperature falls back below the 125°C trip point.

No-Load Stability

The LDOs in the AAT2504 are designed to maintain output voltage regulation and stability under operational no-load conditions. This is an important characteristic for applications where the output current may drop to zero.

Reverse Output-to-Input Voltage Conditions and Protection

Under normal operating conditions, a parasitic diode exists between the output and input of the LDO regulator. The input voltage should always remain greater than the output load voltage maintaining a reverse bias on the internal parasitic diode. Conditions where V_{OUT} might exceed V_{IN} should be avoided since this would forward bias the internal parasitic diode and allow excessive current flow into the V_{OUT} pin, possibly damaging the LDO regulator. In applications where there is a possibility of V_{OUT} exceeding V_{IN} for brief amounts of time during normal operation, the use of a larger value C_{IN} capacitor is highly recommended. A larger value of C_{IN} with respect to C_{OUT} will effect a slower C_{IN} decay rate during shutdown, thus preventing V_{OUT} from exceeding V_{IN}. In applications where there is a greater danger of V_{OUT} exceeding V_{IN} for extended periods of time, it is recommended to place a Schottky diode across V_{IN} to V_{OUT} (connecting the cathode to V_{IN} and anode to V_{OUT}). The Schottky diode forward voltage should be less than 0.45V.

Thermal Considerations and High Output Current Applications

The LDOs of the AAT2504 are designed to deliver continuous output load currents of 300mA each under normal operation. This is desirable for circuit applications where there might be a brief high in-rush current during a power-on event.

The limiting characteristic for the maximum output load current safe operating area is essentially package power dissipation and the internal preset thermal limit of the device. In order to obtain high operating currents, careful device layout and circuit operating conditions need to be taken into account.

The following discussions will assume the LDO regulator is mounted on a printed circuit board utilizing the minimum recommended footprint as stated in the layout considerations section of this document. At any given ambient temperature (T_A), the maximum package power dissipation can be determined by the following equation:

$$P_{D(MAX)} = \frac{T_{J(MAX)} - T_A}{\theta_{JA}}$$

Constants for the AAT2504 are $T_{J(MAX)}$ (the maximum junction temperature for the device, which is 125°C) and θ_{JA} = 50°C/W (the package thermal resistance). Typically, maximum conditions are calculated at the maximum operating temperature of T_A = 85°C and under normal ambient conditions where T_A = 25°C. Given T_A = 85°C, the maximum package power dissipation is 800mW. At T_A = 25°C, the maximum package power dissipation is 2W.

The maximum continuous output current for the AAT2504 is a function of the package power dissipation and the input-to-output voltage drop across the LDO regulator. To determine the maximum output current for a given output voltage, refer to the following equation. This calculation accounts for the total power dissipation of the LDO regulator, including that caused by ground current.

$$P_{D(MAX)} = [(V_{IN} - V_{OUTA})I_{OUTA} + (V_{IN} \cdot I_{GND})] + [(V_{IN} - V_{OUTB})I_{OUTB} + (V_{IN} \cdot I_{GND})]$$

Layout

The suggested PCB layout for the AAT2504 is shown in Figures 1 and 2. The following guidelines should be used to help ensure a proper layout.

1. The input capacitors (C4, C7, C8, and C9) should connect as closely as possible to VIN, VLDOA, VLDOB, VP, and PGND.
2. The output capacitor (C5, and C6) of the LDOs connect as closely as possible to OUT. C2 and L1 should be connected as closely as possible. The connection of L1 to the LX pin should be as short as possible. Do not make the node small by using a narrow trace. The trace should be kept wide, direct, and short.
3. The feedback trace should be separate from any power trace and connect as closely as possible to the load point. Sensing along a high-current load trace will degrade DC load regulation. Feedback resistors should be placed as closely as possible to VOUT to minimize the length of the high impedance feedback trace. If possible, they should also be placed away from the LX (switching node) and inductor to improve noise immunity.
4. The resistance of the trace from the load return to the PGND should be kept to a minimum. This will help to minimize any error in DC regulation due to differences in the potential of the internal signal ground and the power ground.
5. Ensure all ground pins are tied to the ground plane. No pins should be left floating. For maximum power dissipation, it is recommended that the exposed pad (EP) must be soldered to a good conductive PCB ground plane layer to further increase local heat dissipation.

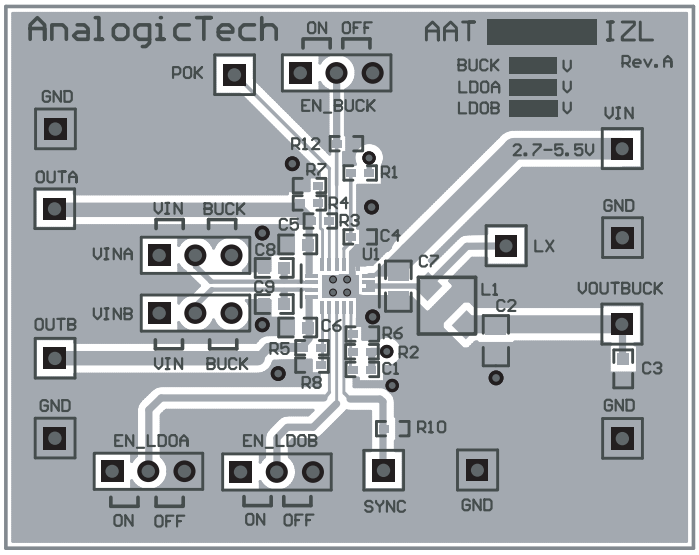


Figure 1: AAT2504 Evaluation Board Top Side Layout.

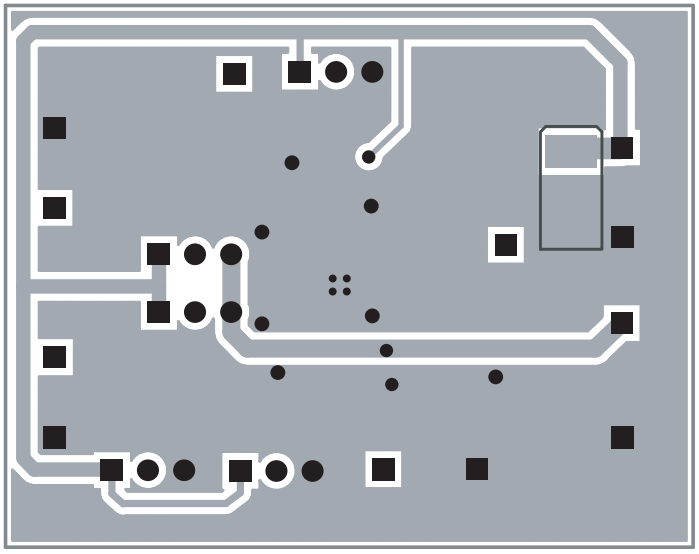
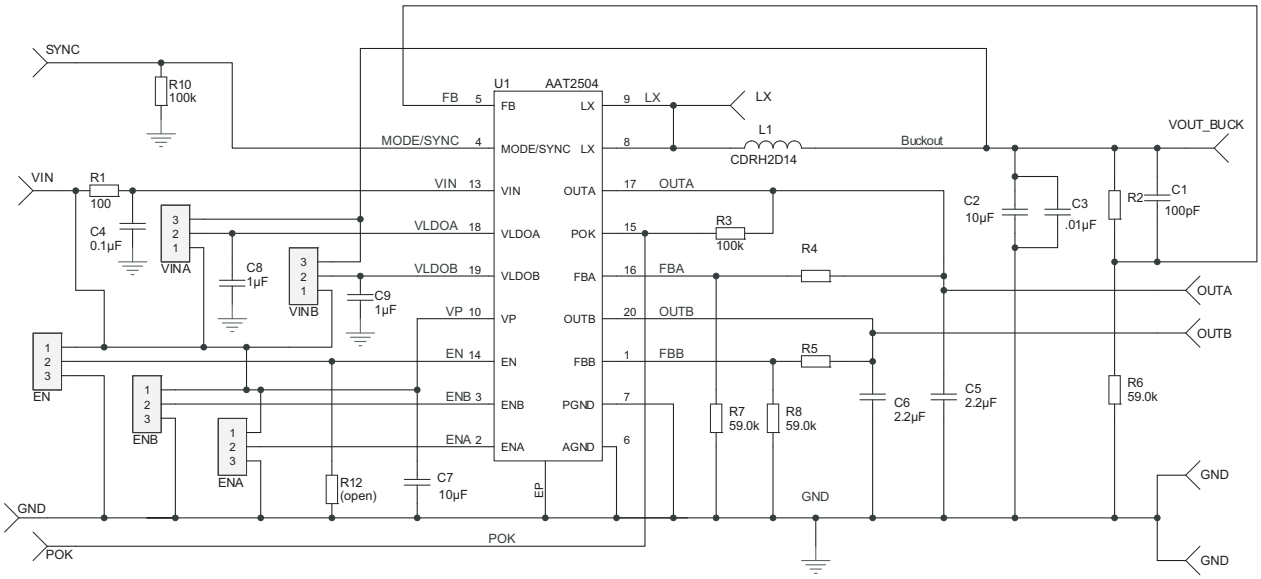


Figure 2: AAT2504 Evaluation Board Bottom Side Layout.



V_{OUT_BUCK} (V)	R2 (kΩ)	L1 (µH)	V_{OUT_LDO} (V)	R4, R5 (kΩ)
0.9	0	1.5	0.8	19.6
1.0	6.65	1.5	0.9	29.4
1.1	13.3	1.5	1.0	39.2
1.2	19.6	1.5	1.1	49.9
1.3	26.1	1.5	1.2	59.0
1.4	32.4	1.5	1.3	68.1
1.5	39.2	2.2	1.4	78.7
1.8	59	2.2	1.5	88.7
1.85	61.9	2.2	1.8	118
2.0	71.5	2.2	1.85	124
2.5	105	3.3	2.0	137
2.8	124	3.3	2.5	187
3.0	137	3.3	3.3	267
3.3	158	3.3		

U1 AAT2504 QFN34-20
L1 Sumida CDRH2D14 or Coltronics SD3812
C2, C7 10uF, 6.3V, X5R, 0805 GRM219R60J106KE19
C5, C6 2.2uF, 10V, X5R, 0603 GRM188R61A225KE34
C8, C9 1uF, 6.3V, X5R, 0603 GRM185R60J105KE26

Figure 3: AAT2504 Evaluation Board Schematic.

Manufacturer	Part Number	Value (µF)	Voltage Rating	Temp. Co.	Case Size
Murata	GRM219R60J106KE19	10	6.3	X5R	0805
Murata	GRM188R60J475KE19	4.7	6.3	X5R	0603
Murata	GRM188R61A225KE34	2.2	10	X5R	0603
Murata	GRM188R61A105KA61	1.0	10	X5R	0603
Murata	GRM185R60J105KE26	1.0	6.3	X5R	0603

Table 4: Surface Mount Capacitors.

Manufacturer	Part Number	Inductance (µH)	Saturated Rated Current (mA)	DCR (mΩ)	Size (mm) LxWxH	Type
Sumida	CDRH2D14-1R5	1.5	1800	63	3.2x3.2x1.55	Shielded
Sumida	CDRH2D14-2R2	2.2	1500	94	3.2x3.2x1.55	Shielded
Sumida	CDRH2D14-3R3	3.3	1200	125	3.2x3.2x1.55	Shielded
Coiltronics	SD3812-1R5	1.5	1580	78	4.0x4.0x1.2	Shielded
Coiltronics	SD3812-2R2	2.2	1320	111	4.0x4.0x1.2	Shielded
Coiltronics	SD3812-3R3	3.3	1100	159	4.0x4.0x1.2	Shielded
Taiyo Yuden	NR3010-1R5	1.5	1200	80	3.0x3.0x1.0	Shielded
Taiyo Yuden	NR3010-2R2	2.2	1100	95	3.0x3.0x1.0	Shielded
Taiyo Yuden	NR3010-3R3	3.3	870	140	3.0x3.0x1.0	Shielded

Table 5: Suggested Inductors and Suppliers.

Ordering Information

Package	Voltage			Marking[1]	Part Number (Tape and Reel)[2]
	Channel 1	Channel 2	Channel 3		
QFN34-20	0.9V	0.6V	0.6V	XWXYY	**AAT2504IZL-BAA-T1**

Pb-free

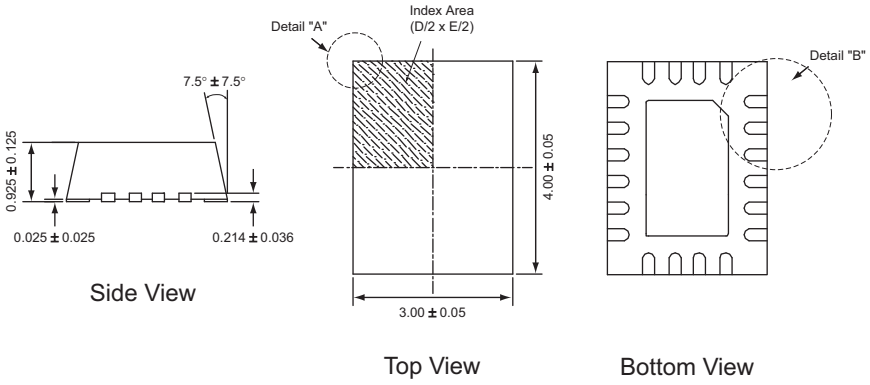
All AnalogicTech products are offered in Pb-free packaging. The term "Pb-free" means semiconductor products that are in compliance with current RoHS standards, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. For more information, please visit our website at http://www.analogictech.com/about/quality.aspx.

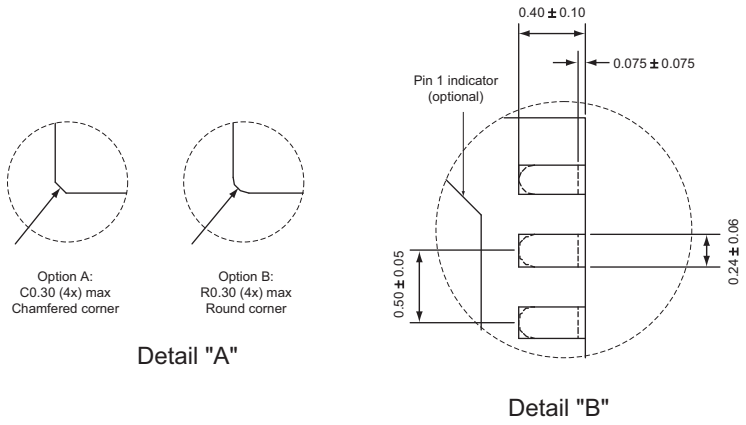
Legend	
Voltage	**Code**
Adjustable (0.6V)	A
0.9	B
1.2	E
1.5	G
1.8	I
1.9	Y
2.5	N
2.6	O
2.7	P
2.8	Q
2.85	R
2.9	S
3.0	T
3.3	W
4.2	C

1. XYY = assembly and date code.
2. Sample stock is generally held on part numbers listed in **BOLD**.

Package Information

QFN34-20





All dimensions in millimeters.

1. The leadless package family, which includes QFN, TQFN, DFN, TDFN and STDFN, has exposed copper (unplated) at the end of the lead terminals due to the manufacturing process. A solder fillet at the exposed copper edge cannot be guaranteed and is not required to ensure a proper bottom solder connection.

Advanced Analogic Technologies, Inc.
3230 Scott Boulevard, Santa Clara, CA 95054
Phone (408) 737-4600
Fax (408) 737-4611