

Low-Noise Step-Up Current Mode PWM Converter



General Description

The FP6290H is a current mode boost DC-DC converter. Its PWM circuitry with built-in 0.15Ω power MOSFET makes this converter highly power efficiently. Selectable high switching frequency allows faster loop response and easy filtering with a low noise output. The non-inverting input its error amplifier is connected to an internal 1.24V precision reference voltage. Soft-Start time can be programmed with an external capacitor, which sets the input current ramp rate. Current mode control and external compensation network make it easy and flexible to stabilize the system.

The FP6290H is available in the SOP-8L (EP) and DFN-8L (EP) package. Combined with low ESR capacitors, it reduced PCB space for step-up applications.

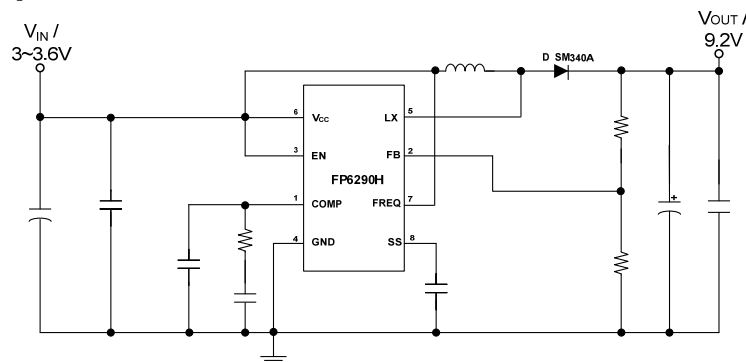
Features

- Adjustable Output from V_{CC} to 12V
- Internal Fixed PWM Frequency: 640KHz / 1.2MHz
- Frequency Selection Pin
- Precision Feedback Reference Voltage: 1.24V
- Internal 0.15Ω, 3A, 14V Power MOSFET
- External Programmable Soft-Start Function (SS)
- Shutdown Current : 0.1μA
- Over Current Protection
- Package: SOP-8L (EP), DFN-8L(EP)

Applications

- LCD Displays
- Digital Cameras
- Handheld Devices
- Portable Products

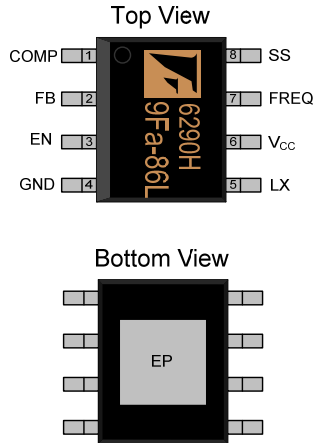
Typical Application Circuit



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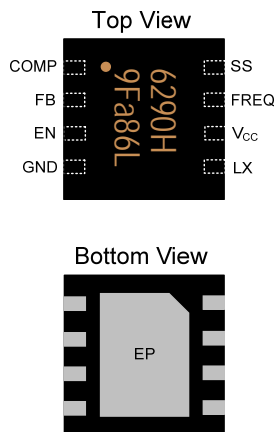
Pin Descriptions

SOP-8L (EP)



Name	No.	I / O	Description
COMP	1	O	Error Amplifier Compensation Output
FB	2	I	Error Amplifier Inverting Input
EN	3	I	Enable Control
GND	4	P	IC Ground
LX	5	O	Switch Output
V _{CC}	6	P	IC Power Supply
FREQ	7	O	Frequency Selection
SS	8	I	Soft-Start Control
EP	9	P	Exposed PAD. Must connect to GND

DFN-8L (EP)

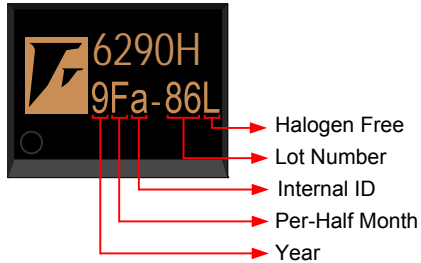


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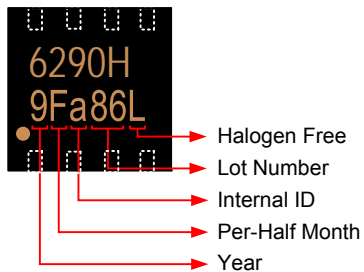
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Marking Information

SOP-8L (EP)



DFN-8L (EP)



Halogen Free: Halogen free product indicator

Lot Number: Wafer lot number's last two digits

For Example: 132386TB → 86

Internal ID: Internal Identification Code

Per-Half Month: Production period indicated in half month time unit

For Example: January → A (Front Half Month), B (Last Half Month)

February → C (Front Half Month), D (Last Half Month)

Year: Production year's last digit

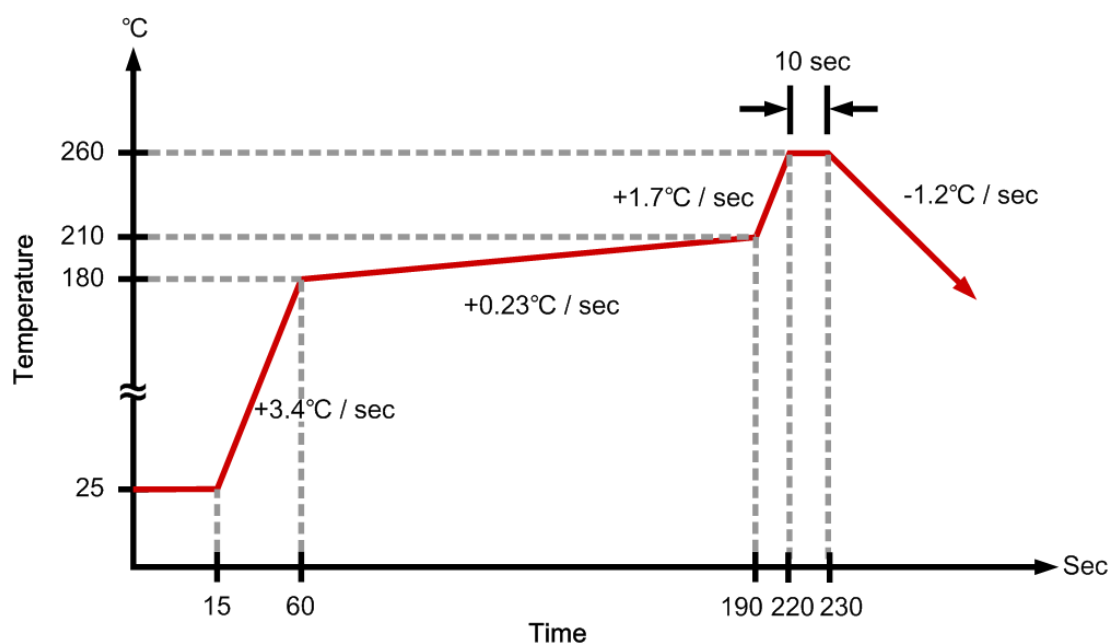
Ordering Information

Part Number	Operating Temperature	Package	MOQ	Description
FP6290HXR-G1	-40°C ~ +85°C	SOP-8L (EP)	2500EA	Tape & Reel
FP6290HdR-G1	-40°C ~ +85°C	DFN-8L (EP)	2500EA	Tape & Reel

Absolute Maximum Ratings

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Supply Voltage	V_{CC}				6	V
LX to GND			-0.3		14	V
SS,COMP to GND			-0.3		$V_{CC}+0.3$	V
EN,FREQ,FB to GND			-0.3		V_{CC}	V
Junction Temperature	T_J				+150	°C
Storage Temperature	T_S		-65		+150	°C
Thermal Resistance	θ_{JA}	SOP-8L (EP)			+60	°C / W
	θ_{JC}				+4	°C / W
	θ_{JA}	DFN-8L (EP)			+68	°C / W
	θ_{JC}				+4.2	°C / W
Lead Temperature		(soldering, 10 sec)			+260	°C

Suggested IR Re-flow Soldering Curve



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Recommended Operating Conditions

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Supply Voltage	V_{IN}		2.6		5.5	V
Operating Temperature			-40		+85	°C

DC Electrical Characteristics ($V_{IN}=3V$, $T_A=25^\circ C$, $V_{FREQ}=0V$, unless otherwise noted)

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Reference Section						
Output Voltage	V_{REF}	COMP connected to FB	1.222	1.240	1.258	V
Line Regulation	$\frac{\Delta V_{REF}}{V_{REF}}$	$V_{CC}=2.6V \sim 5.5V$		0.05		% / V
Output Voltage Change with Temperature		$T_A=-40^\circ C$ to $25^\circ C$		1		%
		$T_A=25^\circ C$ to $85^\circ C$		1		%
Under Voltage Lockout Section						
Upper Threshold Voltage (V_{CC})	V_{UPPER}	$T_A=25^\circ C$		2.38	2.53	V
Lower Threshold Voltage (V_{CC})	V_{LOW}			2.33	2.48	V
Hysteresis (V_{CC})	V_{HYS}			50		mV
Soft-Start Section						
Reset Switch Resistance	R_{SS}				100	Ω
Input Source Current	I_{SS}	$V_{SS}=1.2V$	1.5	4.0	7.0	μA
Oscillator Section						
Frequency	f_{osc}	FREQ=GND	540	640	740	KHz
		FREQ= V_{CC}	1.00	1.22	1.50	MHz
Frequency Change with Voltage	$\frac{\Delta f}{\Delta V}$	$V_{CC}=2.6V$ to $5.5V$		2		% / V
Frequency Change with Temperature	$\frac{\Delta f}{\Delta V}$	$T_A=-40^\circ C$ to $85^\circ C$		10		%
Maximum Duty Cycle	T_{DUTY}	FREQ=GND	79	88		%
		FREQ= V_{CC}		88		%
Error-Amplifier Section						
FB Input Bias Current	I_{BIAS}	$V_{FB}=1.24V$			40	nA
Trans-conductance	gm	$\Delta I=5\mu A$	70	140	240	$\mu A / V$
Voltage Gain	A_V			700		V / V
Output Section						
NMOS Current Limit	I_{LIM}	$V_{FB}=1V$, Duty Cycle=65%		3		A
NMOS On Resistance	$R_{DS(ON)}$	$I_{LX}=1.2A$		0.15	0.5	Ω
Output Leakage Current	I_{LXOFF}	$V_{LX}=12V$		0.01	20	μA
Current-Sense Trans-Resistance	R_{CS}			0.35		V / A

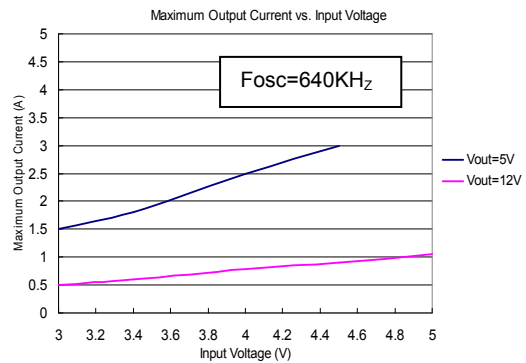
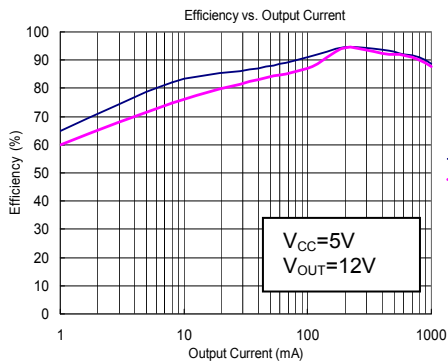
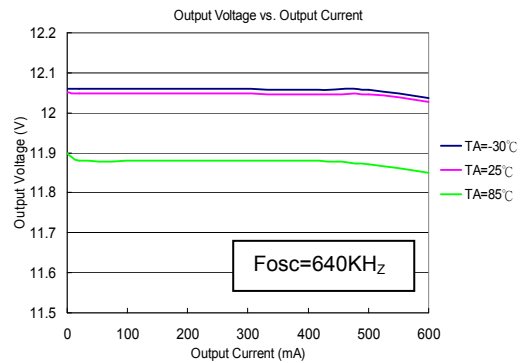
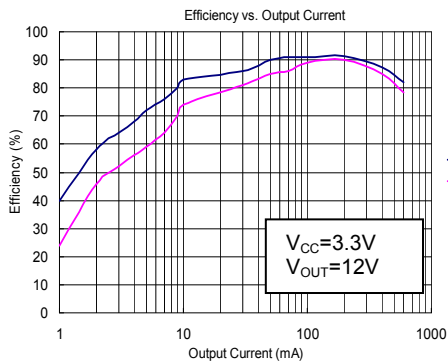
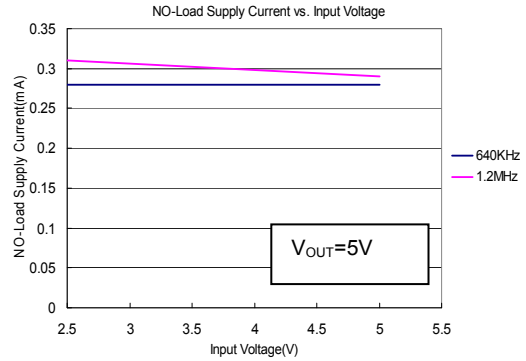
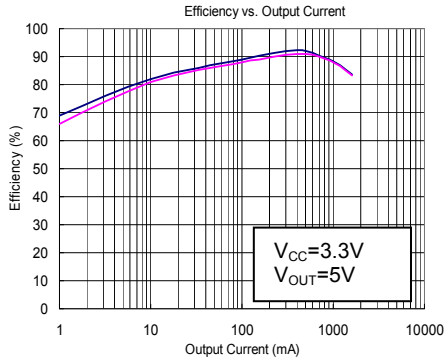
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Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Control Input Section						
Input High Voltage	V_{IH}	EN, FREQ pin $V_{CC}=2.6V\sim 5.5V$	$0.7\times V_{CC}$			V
Input Low Voltage	V_{IL}	EN, FREQ pin $V_{CC}=2.6V\sim 5.5V$			$0.3\times V_{CC}$	V
Hysteresis		EN, FREQ		$0.1\times V_{CC}$		V
FREQ Pull-Down Current	I_{FREQ}		1.8	5	9	μA
EN Input Current	I_{EN}			1		nA
Total Device						
Disable Supply Current	$I_{DISABLE}$	EN=GND		0.1	10	μA
Standby Supply Current	I_{SBY}	$V_{FB}=1.3V$		0.20	0.35	mA
Average Supply Current	I_{AVG}	$V_{FB}=1.0V$		2.0	5.0	mA

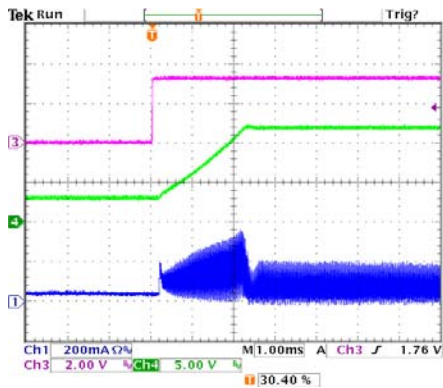
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Typical Operating Characteristics

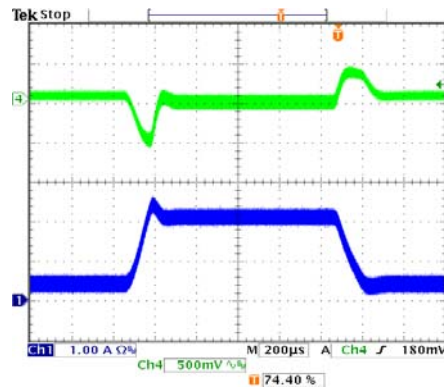
($V_{CC}=3.3V$, $V_{OUT}=5V$, $T_A=25^\circ C$, unless otherwise noted)



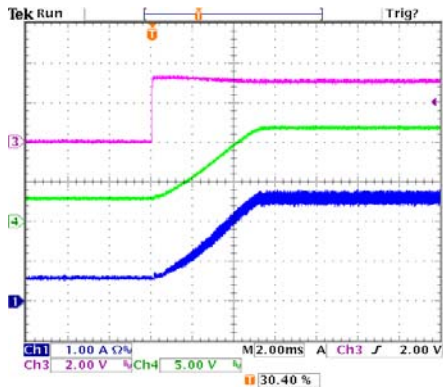
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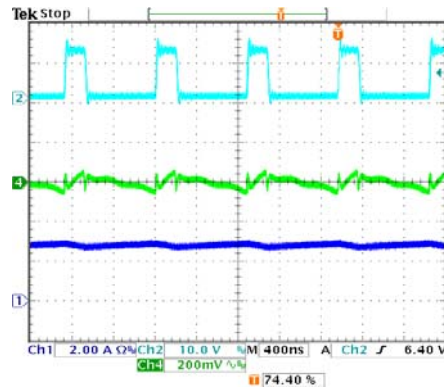
CH1=Inductor Current, CH4= V_{OUT}
 $V_{CC}=3.3V$, $V_{OUT}=12V$
 $I_{LOAD}=10mA$
 Frequency=640KHz



CH1=Inductor Current, CH3=EN, CH4= V_{OUT}
 $V_{CC}=3.3V$, $V_{OUT}=12V$
 $I_{LOAD}=100mA \sim 500mA$
 Frequency=640KHz



CH1=Inductor Current, CH3=EN, CH4= V_{OUT}
 $V_{CC}=3.3V$, $V_{OUT}=12V$
 $I_{LOAD}=600mA$
 Freq=640KHz



CH1=Inductor Current, CH3=LX, CH4= V_{OUT}
 AC-Coupled
 $V_{CC}=3.3V$, $V_{OUT}=12V$
 $I_{LOAD}=600mA$
 Freq=1.2MHz

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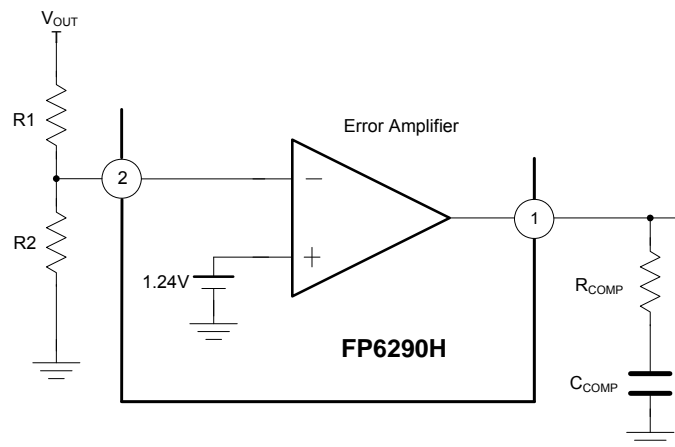
Voltage Reference

A 1.24V reference regulator supplies to the FP6290H error amplifier's non-inverting terminal.

Error Amplifier

The error amplifier compares a sample of the dc-dc converter output voltage with the 1.24V (V_{REF}) reference and generates an error signal for the PWM comparator. Output voltage of dc-dc converter is setting with the resistor divider by the following equation:

$$V_{OUT} = \left(1 + \frac{R1}{R2}\right) \times 1.24$$



Oscillator

The switching frequency of FP6290H can be selected to operate at either 640KHz or 1.2MHz. Connect the FREQ pin to GND for 640KHz operation, or V_{CC} for 1.2MHz operation. FREQ pin has an internal pull-down current around $5 \mu A$. It gives user the option of selecting 640KHz operation by leaving FREQ unconnected.

Soft Start

The soft start is functional after power on. The interval of soft start time is determined by a capacitor connected to SS pin. When EN pin is taken high, the soft start capacitor (C_{SS}) is charged by a constant current of $4 \mu A$ (typ). During this interval, the SS voltage directly controls the peak inductor current. The maximum load current is available after the soft-start interval is completed. Once the EN pin is taken low, the soft-start capacitor is discharged to ground to prepare for next start-up.

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The load must wait for the soft-start interval to finish before drawing a significant amount of load current. The duration after which the load can begin to draw maximum load current is:

$$T_{MAX} = 6.77 \times 10^5 C_{SS}$$

EN

The FP6290H can be turned off to reduce the supply current to $0.1 \mu A$ when EN is low. In this mode, the internal reference, error amplifier, comparators, and biasing circuitry turn off while the N-channel MOSFET is turned off. The boost converter's output is connected to V_{CC} by the external inductor and catch diode.

Output Current Capability

The output current capability of the FP6290H is a function of current limit, input voltage, operation frequency, and inductor value. Because of the slope compensation used to stabilize the feedback loop, the duty cycle affects the current limit. The output current capability is governed by the following equation:

$$I_{OUT(MAX)} = [I_{LIM} \times (1.26 - 0.4 \times \text{Duty}) - 0.5 \times \text{Duty} \times V_{IN} / (f_{osc} \times L)] \times \eta \times V_{IN} / V_{OUT}$$

Where:

I_{LIM} = current limit specified at 65%

$$\text{Duty} = \text{duty cycle} = \frac{(V_{OUT} - V_{IN} + V_{DIODE})}{V_{OUT} - I_{LIM} \times R_{ON} + V_{DIODE}}$$

V_{DIODE} = catch diode forward voltage at I_{LIM}

η = conversion efficiency, 85% nominal

Current Limitation

The internal power-MOS switch current is monitored cycle-by-cycle and is limited to the value not exceed 3A (Typ.). When the switch current reaches the limited value, the internal power-MOS is turned off immediately until the next cycle.

Typical Application

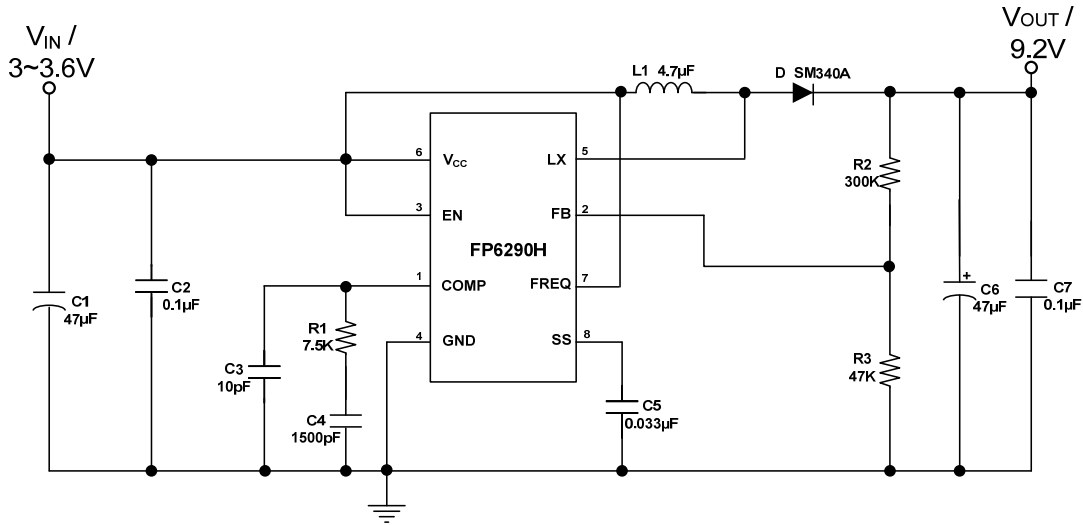


Figure 1 Typical Application Circuits

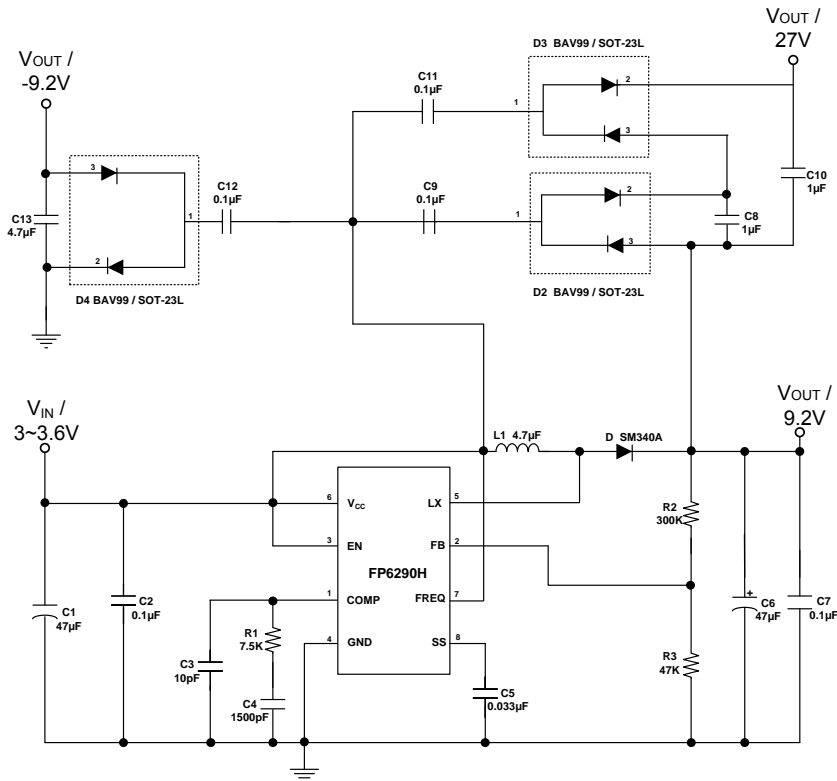
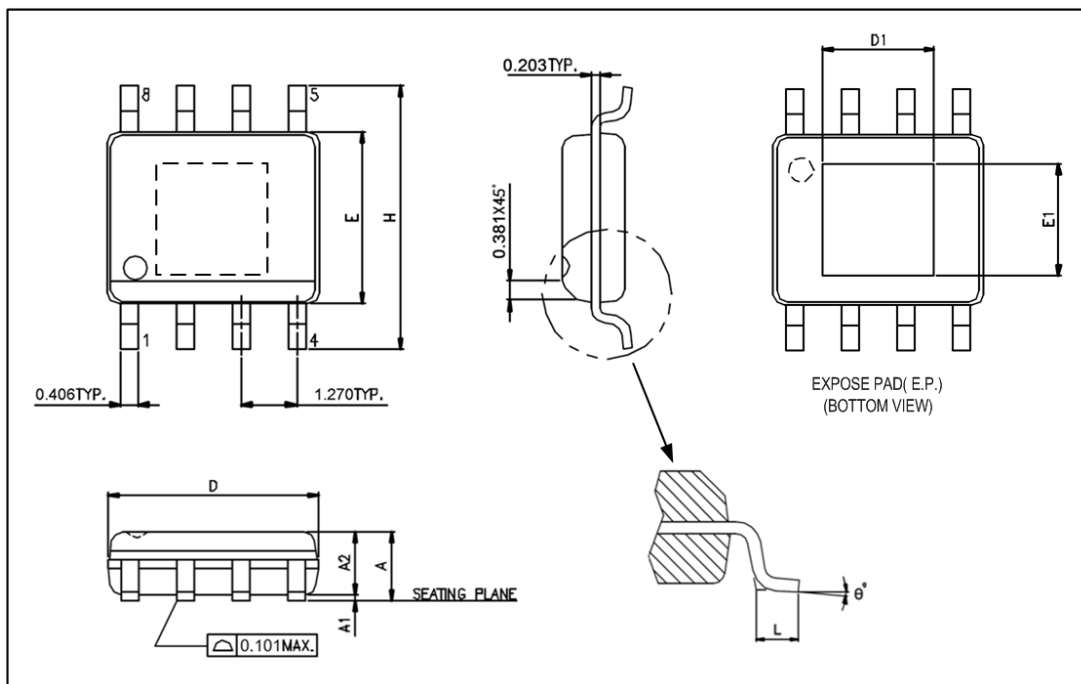


Figure 2 TFT Panel Power Supply Application Circuits

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Package Outline

SOP-8L (EP)



UNIT: mm

Symbols	Min. (mm)	Max. (mm)
A	1.346	1.752
A1	0.050	0.152
A2		1.498
D	4.800	4.978
E	3.810	3.987
H	5.791	6.197
L	0.406	1.270
θ°	0°	8°

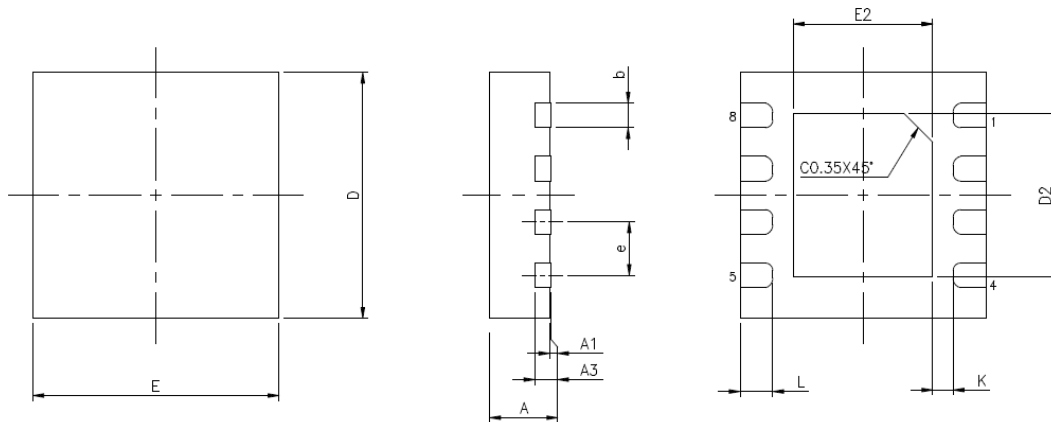
Exposed PAD Dimensions:

Symbols	Min. (mm)	Max. (mm)
E1		2.184 REF
D1		2.971 REF

Note:

1. Package dimensions are in compliance with JEDEC outline: MS-012 AA.
2. Dimension "D" does not include molding flash, protrusions or gate burrs.
3. Dimension "E" does not include inter-lead flash or protrusions

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DFN-8L (EP)


Symbols	Min. (mm)	Max. (mm)
A	0.700	0.800
A1	0.000	0.050
A3	0.20REF	
b	0.25	0.35
D	3.00	
E	3.00	
D2	1.600	2.500
E2	1.350	1.750
e	0.650	
L	0.300	0.500
K	0.200	-

UNIT: mm

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